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GP2818
04.292

To: Commissioner of Patents and Trademarks
    Washington, D.C.   20231

Fr: George O. Saile,   Reg. No. 19,572
    20 McIntosh Drive
    Poughkeepsie, N.Y. 12603

Subject:

| Serial No.   10/076,826   02/15/02

Peter W. Lee et al.

BIT-BY-BIT VT-CORRECTION OPERATION
FOR NONVOLATILE SEMICONDUCTOR ONE-
TRANSISTOR-CELL, NOT-TYPE FLASH
EEPROM

| Grp. Art Unit: 2818 |
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INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
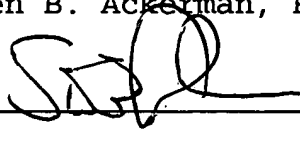
In An Application.

The following Patents and/or Publications are submitted to

comply with the duty of disclosure under CFR 1.97-1.99 and

37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on April 10 , 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date _____ 4/10/02

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U.S. Patent 5,748,538 to Lee et al., "OR-Plane Memory Cell Array for Flash Memory with Bit-Based Write Capability and Methods for Programming and Erasing the Memory Cell Array," describes Flash memory architectures and a method of over erase repair.
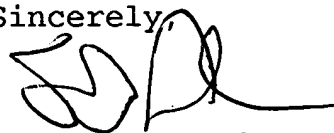
U.S. Patent 5,848,000 to Lee et al., "Flash Memory Address Decoder with Novel Latch Structure," discloses a flash memory address decoder circuit with a novel latch structure.

U.S. Patent 5,237,535 to Mielke et al., "Method of Repairing Overerased Cells in a Flash Memory," teaches the method to repair over erased cells in a Flash memory.

U.S. Patent 6,122,198 to Haddad et al., "Bit by Bit APDE Verify for Flash Memory Applications," discloses a method to erase, bit-by-bit erase verify, over erase verify, and over erase correct.

U.S. Patent 5,822,252 to Lee et al., "Flash Memory Wordline Decoder with Overerase Repair," discloses the use of a negative voltage on a non-selected wordline.

Sincerely,

Stephen B. Ackerman, Reg. #37761